|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Course No | | Course Name | L-T-P-Credits | |
| **EE 218** | | **Digital logic design** | **3-0-0: 3** | |
| Prerequisite: nil; Co requisite: nil | | | | |
| **Course Objectives**:   1. To find out the simplest expression using Boolean algebra, K-map and Quine Mclusky method. 2. To understand the circuit operation of any logic gate. 3. To understand and design logic circuit for combinational and sequential operation. 4. To understand and implement logic circuit to generate desired signal. | | | | |
| **SYLLABUS** | | | | |
| **Module** | **Contents** | | | **Hours** |
| I | **Boolean algebra and switching functions**  Basic Logic Operation and Logic Gates, Truth Table, Basic Postulates and Fundamental Theorems of Boolean Algebra, Standard Representations of Logic Functions- SOP and POS Forms, Simplification of Switching Functions-K-Map and Quine-Mccluskey Tabular Methods, Synthesis of Combinational Logic Circuits. | | | 08 |
| II | **Combinational logic circuits using msi integrated circuits**  Adder, Subtractor, BCD Adder, Parallel Binary Adder, Look Ahead Carry Adder, Encoder, Decoder, Multiplexer and Demultiplexer Circuits, Code converter, BCD-To-Segment Decoder, 7-Segment Displays. | | | 08 |
| III | **Introduction to flip-flops**  Basic Concepts of Sequential Circuits, Cross Coupled SR Flip-Flop Using NAND or NOR Gates, JK Flip-Flop Rise Conditions, Clocked Flip-flops, D-Types and Toggle Flip-flops, Truth Tables and Excitation Tables for Flip-flop. Master Slave Configuration, Edge Triggered and Level Triggered Flip-flop, Elimination of Switch Bounce using Flip-flop, Flip-flop with Preset and Clear. | | | 07 |
| IV | **Sequential logic circuit design**  Introduction to State Machine, Mealy and Moore Model, State Machine Notation, State Diagram, State Table, Transition Table, Table Excitation, Table and Equation, Basic Concepts of Counters and Register, Binary Counters, BCD Counters, Up Down Counter, Johnson Counter, Module-N Counter, Design of Counter using State Diagrams and Tables, Sequence Generators, Shift Left and Right Register, Registers with Parallel Load, Serial -in-Parallel-Out(SIPO) and Parallel-In-Serial-Out(PISO), Register Using Different Types of Flip-flop. | | | 08 |
| V | **Digital logic families**  Digital IC Terminology, Transistor-Transistor Logic(TTL), Integrated Injection Logic(I2L), Emitter Coupled Logic (ECL), Metal Oxide Semiconductor(MOS) Logic, Complementary Metal oxide semiconductor (CMOS) Logic. | | | 05 |

**Essential Readings:**

1. Floyed Thomas L., Digital Fundamentals, Pearson Education, 11th edition, 2014.

**Supplementary Readings:**

1. Kumar Anand, ‘Fundamentals of Digital Circuits’, Prentice Hall India Learning Private

Limited; 2 edition, 2009.

2. Morris Mano,M .'Digital logic and computer design', Prentice Hall of India, 2005.

3. Donald D. Givone, “Digital Principles and Design”, Tata McGraw Hill, 2002.

4. Tocci R.J.,Neal S. Widmer, 'Digital Systems: Principles and Applications', Pearson Education

Asia, Second Indian Reprint, 2002

5. Donald P Leach ,Albert Paul Malvino,Goutam Sha,”Digital Principles and Applications”The

McGraw –Hill ,sixth edition, 2007