			National Institute of Technology Meghalaya An Institute of National Importance														CURRICULUM	
Pi	ogramr	ne I	Bachelor of Technology in Computer Science and Engineering									Year of Regulation				2019-2020		
D	epartme	ent (Computer Science and Engineering										Semester				V	
Cou	urse				Co	ourse Nam	1e				Credit Structure			1	Marks Distribution			
				_						L	Т	P	C	INT	MID	END	Total	
CS	321	To under	stand the	For	mal Verit	ication	ormal verifi	cation		3	0	0 Able to u	3 nderstand	50 the fundam	50 ental conce	100 apt of formation	200 al	
				runuu							CO1	verification						
Course Objectives		To demonstrate the modeling of sequential systems, linear time properties, linear temporal logic, computation tree logic, model checking CTL and model checking LTL								Course Outcomes	CO2	Able to demonstrate the modeling of sequential systems, linear time properties, linear temporal logic						
		To explain binary decision diagrams, symbolic model checking, model checking with SAT, bounded model checking, craig interpolation									CO3	Able to explain computation tree logic, model checking CTL and model checking LTL						
		To understand decision procedures in model checking, practical industrial-scale verification									CO4	Able to demonstrate binary decision diagrams, symbolic model checking						
											CO5	Able to demonstrate model checking with SAT, bounded model checking, craig interpolation						
											CO6	Able to explain decision procedures in model checking, practical industrial-scale verification						
Na	Mapping with Program Outcomes (POs)									Mapping with PSOs								
INO.	COS	PO1	PC)2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	
1	CO1	3	3		0	0	0	0	0	0	2	0	0	0	3	0	3	
2	CO2	3	3		3	1	2	0	0	0	1	0	0	0	2	3	2	
3	CO3	1	2		3	3	2	2	0	0	0	0	0	0	2	3	3	
4	CO4	1	2		3	3	3	2	3 2	0	2	0	0	1	2	ن ۲	2	
5 6	CO3	1	2		3	2	3	2	2	0	2	0	0	1	2	3	2	
						-	-	-	SYLLA	BUS			-		_	-		
No.							(Content							Hours		COs	
I	Introd	troduction to Formal Verification														2 CO1		
II	Modelling sequential systems as labelled transition systems (Kripke structures), Linear time properties, Linear temporal logic (LTL).														06	06 CO2		
III	Comp	Computation tree logic (CTL) and CTL * , Model checking CTL , Model checking LTL														06 CO3		
IV	Counterexamples and witnesses, Binary decision diagrams (BDD), Symbolic model checking														06	06 CO4		
V	Model interp	checkin olation	g with S	SAT, I	bounded	I model cl	hecking,	Complete	eness th	nresholds a	nd k-ind	uction, C	raig		08	8 CO5		
VI	Equiva prese	alences nt challe	and abs nges	tracti	ions, Dec	cision pro	ocedures	in model	checkii	ng, Practica	al, indust	rial-scale	e verificat	ion,	08	B CO6		
							To	tal							36			
Esse	ntial Re	adings												I		L		
1.	Principle	es of Mod	el Checki	ng, by	C. Baiera	nd JP. Ka	toen, The I	MIT Press, 2	2008 edi	tion.	-nd							
2.	Model C	hecking,	by Edmui	nd M.	Clarke, Jr.	, Orna Gru	mberg, and	d Doron A. I	Peled, T	he MIT Press,	2 [™] editic	on, 2000.		and				

Supplementary Readings

1. Introduction to Formal Hardware Verification, by Thomas Kropf, Springer, 1999 edition.

2. Formal Hardware Verification: Methods and Systems in Comparison, Ed. by Thomas Kropf, Springer, 1997 edition.

3. Advanced Formal Verification, by Rolf Drechsler, Springer, 2004 edition.