	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 518	**LOW POWER VLSI DESIGN**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives	Preliminaries on Power dissipation	Course Outcomes	CO1	Able to understand basics of Power Dissipation.
	Fundamentals of low power circuits.		CO2	Able to learn low power circuit design.
	Basic synthesis for low power circuits.		CO3	Able to do circuit level optimization.
	Basics of SRAM memory		CO4	Able to acquire knowledge on SRAM.
	Basics of design and test of low voltage circuits		CO5	Able to design low power circuits at submicron level.

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**3**	**0**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**3**	**0**	**0**
2	CO2	**3**	**3**	**3**	**1**	**0**	**0**	**0**	**0**	**2**	**0**	**0**	**0**	**2**	**0**	**0**
3	CO3	**2**	**3**	**3**	**1**	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**2**	**3**	**3**
4	CO4	**2**	**2**	**3**	**0**	**2**	**2**	**3**	**0**	**2**	**0**	**0**	**1**	**2**	**3**	**2**
5	CO5	**2**	**2**	**0**	**0**	**2**	**2**	**3**	**0**	**2**	**0**	**0**	**1**	**3**	**3**	**0**

SYLLABUS

No.	Content	Hours	COs
I	Physics of Power Dissipation in CMOS FET Devices Physics of power dissipation in MOSFET devices, power dissipation in cmos, low power vlsi design: Limits	5	CO1 CO1 CO1 CO1
II	Power Estimation Modeling in signals, Signal Probability calculation, Probabilistic Techniques for signal activity estimation, Statistical Techniques, Estimation of Glitching power, Sensitivity Analysis. Power estimation using the input vector compaction, power dissipation in domino cmos, high level power estimation, Information theory based approaches, Estimation of maximum power.	7	CO2 CO2 CO2 CO2
III	Synthesis for Low Power Behavioral Level Transforms, Logic Level Optimization for Low power, Circuit Level Optimization.	6	CO2 CO2 CO3 CO3
IV	Design and Test of Low Voltage CMOS Circuits Circuit Design style, Leakage current in deep submicrometer transistors, Deep submicrometer device design issues, Key to minimizing SCE, Low voltage circuit design techniques, Designing deep submicrometer ics with elevated intrinsic leakage, multiple supply voltages.	7	CO3 CO3 CO3 CO3
V	Low Power Static RAM Architectures Organization of a static RAM, MOS Static RAM Memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in write driver circuits, Reducing power in sense amplifier circuits, method for achieving low core voltages from a single supply.	6	CO4 CO4 CO4 CO4
VI	Low Energy Computing using Energy Recovery Techniques Energy dissipation in transistor channel using an RC model, Energy recovery circuit design, Designs with partially reversible logic, Supply clock generation.	5	CO2 CO2 CO2 CO2
Total Hours		36	

Essential Readings

1. K. Roy and S. C. Prasad, Low Power CMOS VLSI Circuit Design, John Wiley and Sons, 3rd Edition, 2009.
2. Jan Rabaey, Low Power Design Essentials, Springer Publications, 1st Edition, 2009.
3. Chandrakasan and R. Brodersen, Low-Power CMOS Design, IEEE Press, 1st Edition, 1995.

Supplementary Readings

1. Chandrakasan, Bowhill, and Fox, Design of High-Performance Microprocessors, IEEE Press, 1st Edition, 2000.
2. G. Yeap, Practical Low Power Digital VLSI Design, Springer Publications, 1st Edition, 1995.