<table>
<tr><td rowspan="2"></td><td rowspan="2" colspan="6" align="center">National Institute of Technology Meghalaya
An Institute of National Importance</td><td colspan="2" align="center">CURRICULUM</td></tr>
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		National Institute of Technology Meghalaya An Institute of National Importance			**CURRICULUM**

Programme	**M.Tech/Ph.D**	Year of Regulation	**2021-22**
Department	**Electronics and Communication Engineering**	Semester	**I**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 521	**Electronic System Design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes	
Design of LSI and MSI circuits		CO1	Able to design and optimize various Electronics circuits
Design and optimize the VLSI & controllers Circuits		CO2	Able to design and analyse Sequential and parallel circuits
Design fault free circuits		CO3	Able to detect faults and design free fault circuits
Implement the circuits using FPGA and ASIC		CO4	Able to implement the circuits in FPGA and ASIC

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	2	1	2	0	1	0	0	0	0	0	0	0	2	0	1	0
2	CO2	1	2	2	2	0	0	0	0	0	0	0	1	2	1	2	0
3	CO3	0	2	2	1	2	0	0	0	0	0	0	2	2	1	2	0
4	CO4	0	2	0	1	2	0	0	0	0	0	0	2	2	2	2	0

<div align="center">SYLLABUS</div>

No.	Content	Hours	COs
I	**MSI and LSI Circuits and Their Applications** Arithmetic Circuits, Comparators, Multiplexers, Code Converters, XOR And AND-OR INVERTER Gates, Wired Logic, Bus Oriented Structures, Tri-State Bus System, Propagation Delay.	8	CO1
II	**Sequential Machines** The Concept Of Memory, The Binary Cell, The Cell And The Bouncing Switch, Set I Reset, D, Clocked T, Clocked JK Flip Flop, Design Of Clock FIF, Conversion, Clocking Aspects, Clock Skew, State Diagram Synchronous Analysis Process, Design Steps For Traditional Synchronous Sequential Circuits, State Reduction, Design Steps For Next State Decoders, Design Of Out Put Decoders, Counters, Shift Registers and Memory.	10	CO1 CO2
III	**Multi input System Controller Design** System Controllers, Design Phases And System Documentation, Defining The System, Timing And Frequency Considerations, Functional, Position And Detailed Flow Diagram Development, MDS Diagram, Generation, Synchronizing Two System And Choosing Controller, Architecture, State Assignment, Next State Decoders And Its Maps, Output Decoders, Clock And Power Supply Requirements, MSI Decoders, Multiplexers In System Controllers, Indirect Addressed Multiplexers Configurations, Programmable System Controllers, ROM, PLA And PAL Based Design. Introduction to the CPLD &FPGA.	10	CO4
IV	**Asynchronous Finite State Machines** Scope, Asynchronous Analysis, Design of Asynchronous Machines, Cycle And Races, Plotting And Reading The Excitation Map, Hazards, Essential Hazards Map Entered Variable, MEV Approaches To Asynchronous Design, Hazards In Circuit Developed By MEV Method.	8	CO3 CO4
	Total Hours	36	

Essential Readings

1. Fletcher, "An Engineering Approach to Digital Design" Prentice-Hall 1980

2. Z. Kohavi, "Switching and Finite Automata Theory", Tata McGraw- Hill 2nd Edition 2008

Supplementary Readings

1. Markovitz, "Introduction to Logic Design", Tata McGraw- Hill 3rd Edition 2009

2. Morris. M.Mano "Digital Design" Prentice-Hall 5th Edition 2015