	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 530	**VLSI DESIGN VERIFICATION AND TESTING**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Understanding verification methodology and testing		CO1	Able to write programme though system Verilog
	Study language fundamentals for verification		CO2	Able to understand language sematics
	Design assertions and Randomization constructs		CO3	Able to design test cases using assertions
			CO4	Able to test the circuits with randomization

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**1**	**1**	**2**	**1**	**2**	**1**	**-**	**-**	**2**	**-**	**2**	**1**	**3**	**3**	**1**
2	CO2	**3**	**3**	**3**	**3**	**-**	**3**	**1**	**-**	**3**	**3**	**-**	**1**	**2**	**3**	**2**
3	CO3	**3**	**3**	**3**	**3**	**2**	**0**	**-**	**1**	**0**	**-**	**1**	**2**	**3**	**1**	**3**
4	CO4	**1**	**2**	**3**	**0**	**2**	**2**	**2**	**-**	**2**	**1**	**-**	**1**	**1**	**1**	**3**

SYLLABUS

No.	Content	Hours	COs
I	Verification guidelines Verification Process, Basic Test-bench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Test-bench components, Layered test-bench, Building layered test-bench, Simulation environment phases, Maximum code reuse, Testbench performance	8	CO1
II	Data types Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.	10	CO2
III	Procedural statements and routines Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.	8	CO2
VI	System Verilog Assertions Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a test bench.	8	CO3
V	Randomization Introduction, What to randomize, Randomization in System Verilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre randomize and post randomize functions, Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration	5	CO4
	Total Hours	39	

Essential Readings

1. C. Spears, System Verilog for Verification, Springer, 2nd Edition, 2010.
2. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, 2004
3. IEEE Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language," in IEEE Std 1800-2017 (Revision of IEEE Std 1800-2012) , vol., no., pp.1-1315, 22 Feb. 2018
4. System Verilog website – www.systemverilog.org

Supplementary Readings

1. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
2. General reuse information and resources www.design-reuse.com
3. OVM, UVM(on top of SV) www.verificationacademy.com Verification IP resources
4. http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
5. http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx.