National Institute of Technology Meghalaya

An Institute of National Importance

CURRICULUM

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**I**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 517	**Device Fabrication & Characterization Technology**	**3**	**0**	**0**	**3**	**25**	**25**	**50**	**100**

Course Objectives		Course Outcomes	
	To learn about clean room, wafer cleaning and wet etching process	CO1	Able to understand clean room, wafer cleaning and wet etching process
	To learn about the impurity incorporation technology	CO2	Able to learn the impurity incorporation technology
	To learn about the oxidation and deposition technology	CO3	Able to learn the oxidation and deposition technology
	To learn about the lithography technology	CO4	Able to acquire knowledge on the lithography technology

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	2	3	2	1	0	3	0	0	2	0	0	0	3	0	3
2	CO2	3	2	0	1	0	0	0	0	2	0	0	0	2	0	2
3	CO3	2	3	3	1	2	0	0	0	0	0	0	0	2	3	0
4	CO4	2	2	3	0	2	2	3	0	2	0	0	1	0	3	2

SYLLABUS

No.	Content	Hours	COs
I	Environment for VLSI Technology: Clean room and safety requirements. Water cleaning processes and wet chemical etching techniques.	5	CO1
II	Impurity Incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; Characterization of Impurity profiles.	7	CO2
III	Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High K and low k dielectrics for ULSI.	8	CO3
IV	Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation. Chemical Vapour Deposition Techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.	8	CO3, CO4
V	Metal Film Deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multilevel metallisation schemes. Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS Technologies.	8	CO3, CO4
	Total Hours	36	

Essential Readings

1. Gary S. May, S. M. Sze, “Fundamentals of Semiconductor Fabrication”, John Wiley Inc. , 2014.
2. S.M. Sze, “VLSI Technology”, McGraw Hill, 2nd ed, 1988.

Supplementary Readings

1. S.K. Ghandhi, “VLSI Fabrication Principles”, John Wiley Inc., New York, 2nd ed, 1994
2. S. Cambell,, “The Science and Engineering of Microelectronic Fabrication”, Oxford University Press., revised ed, 2003.