	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**I**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 519	**CAD for VLSI design**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Learn VLSI Design methodologies		CO1	Outline floor planning and routing
	Understand VLSI design automation tools		CO2	Explain Simulation and Logic Synthesis
	Realize the modelling and simulation and Automation tools		CO3	Discuss the hardware models for high level synthesis
	Design circuits with HLS methodology		CO4	Able to test the larger circuits with automation tools

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**1**	**1**	**2**	**3**	-	-	-	-	-	-	-	**3**	**3**	**1**
2	CO2	**1**	**1**	**1**	**2**	**3**	-	-	-	-	-	-	-	**1**	**2**	**1**
3	CO3	**3**	-	**1**	**2**	**3**	--	-	-	-	-	-	-	**2**	**2**	**3**
4	CO4	**1**	**2**	**1**	**3**	**1**	-	-	-	-	-		-	**1**	**2**	**3**

SYLLABUS

No.	Content	Hours	COs
I	Introduction: VLSI design flow, CMOS based logic design, challenges. Verilog/VHDL: Introduction and use in synthesis, modelling combinational and sequential logic, writing test benches.	6	CO1
II	Logic synthesis: Two-level and multilevel gate-level optimization, state assignment of finite state machines. High-level synthesis: Basic concepts, partitioning, scheduling, allocation and binding. Technology mapping.	12	CO2, CO3
III	Testability issues: Fault modelling and simulation, test generation, design for testability, built-in self-test. Testing SoC's. Basic concepts of verification.	8	CO2
IV	Physical design automation: Review of MOS/CMOS fabrication technology. VLSI design styles: fullcustom, standard-cell, gate-array and FPGA.	2	CO2
V	Physical design automation algorithms: Floor-planning, placement, routing, compaction, design rule check, power and delay estimation, clock and power routing, etc. Special considerations for analog and mixed-signal designs	8	CO4
	Total Hours	36	

Essential Readings

1. J. Bhasker, “Verilog VHDL synthesis: a practical primer”, B S Publications
2. M.D.Ciletti, “Advanced digital design withe the Verilog HDL”, Prentice-Hall of India Pvt. Ltd.
3. D.D. Gajski, N.D. Dutt, A.C. Wu and A.Y. Yin, “High-level synthesis: introduction to chip and system design”, Kluwer Academic Publishers.
4. N.A. Sherwani, “Algorithms for VLSI physical design automation”, Kluwer Academic Publishers.
5. M. Sarrafzadeh and C.K. Wong, “An introduction to physical design”, McGraw Hill

Supplementary Readings

1. S.M. Sait and H. Youssef, “VLSI physical design automation: theory and practice”, World Scientific Pub.
2. R.H. Katz, “Contemporary logic design”, Addison-Wesley Pub.
3. M.J. Sebastian Smith snd A. Wesley, “Application-specific integrated circuits”, Addison-Wesley Pub.
4. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing”, Kluwer Academic Publishers.
5. M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems Testing and Testable Design”, Wiley IEEE Press