	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 528	**RECONFIGURABLE COMPUTING**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Understand various computing platforms		CO1	Able to select suitable hardware FPGA, GPU, DSP, Microcontroller for an application
	Design of SoC system with various peripherals, memory , third party intellectual properties (IP) and buses		CO2	Able to understand the design methodology of micro-processor system on Chip (SoC) buses, memory peripherals on FPGA
	Study various bus protocols and interface with HDL IPs		CO3	Able to evaluate hardware accelerator and achieve acceleration factor for DSP application.
	Develop hardware accelerators in SoC system		CO4	Able to explore DMA, Interrupt and Display controllers in complex application

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**3**	**2**	**2**	**1**	**2**	**1**	**-**	**-**	**2**	**-**	**-**	**1**	**3**	**3**	**1**
2	CO2	**1**	**2**	**1**	**3**	**-**	**-**	**1**	**-**	**3**	**-**	**-**	**1**	**2**	**2**	**1**
3	CO3	**2**	**3**	**3**	**1**	**2**	**0**	**-**	**1**	**0**	**-**	**1**	**2**	**3**	**2**	**1**
4	CO4	**1**	**2**	**3**	**0**	**2**	**2**	**2**	**-**	**2**	**-**	**-**	**1**	**1**	**2**	**3**

SYLLABUS

No.	Content	Hours	COs
I	Introduction to Reconfigurable Computing Introduction to Reconfigurable Computing, Coarse-grained reconfigurable devices, Fine-grained reconfigurable devices. FPGA architecture, FPGA design cycle, Multi FPGA systems, Embedded computer organization and methodology of System on chip (SoC) system in FPGA devices, Design challenges and Differences GPP, DSP, ASIC and FPGA based System On Chip platforms, Application profiling and partitioning, FPGAs vs. Multi-core processor architectures, High level compilation	8	CO1 CO2
II	Emulating SoC Architectures on FPGAs Emphasis on different embedded processors and multiprocessor and architectures. Hardware-software co-design of Embedded Systems, Simple & Autonomous I/O Controllers, Custom Intellectual-Property (IP) and Coprocessor creation, hardware design for System-On-a-Chip; Concepts & types of Memory interfacing, Cache mapping techniques and impact on system performance. Co-simulation using different simulators, system level optimization, and System level design Trade-offs, Power, Energy, Performance and Area. Design for Test.	12	CO2
III	Bus-protocols and Intellectual Property study Architecture exploration of IP, Design of Master and Slave Bus protocols based IPs, Bus protocols AXI. Design Metrics, General purpose peripherals (interrupt, timer, clock, DMA etc.) and special purpose peripherals Serial Transmission protocols & Standards, and advanced high speed buses. Debugging methodologies	12	CO3
VI	Analysis and case-studies Exploration of HLS tools, System Modeling. Models of Computation and System Specification Languages, High Level Computation/Behavioral Synthesis. Advanced concepts. Partial reconfiguration, Dynamic reconfiguration, Application case study like JPEG, H.264	6	CO3 CO4
	Total Hours	38	

Essential Readings

1. R. Sass and A. G. Schmidt. Embedded Systems Design with Platform FPGAs Principles and Practices. Elsevier Inc, USA, 2010.
2. The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Strathclyde Academic Media , UK ,2014
3. S. Hauck and A. DeHon, Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing, Morgan Kaufmann, 2008.
4. Cardoso, João M. P.; Hübner, Michael (Eds.), Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, Springer, 2011.

Supplementary Readings

1. D. Amos, A. Lesea and R. Richter. FPGA-Based Prototyping Methodology Manual Best Practices in Design-for-Prototyping. Synopsys,Inc, Mountain View, CA, USA, 2010.
2. F. Vahid, and T. Givargis, Embedded System Design: A unified Hardware/Software Introduction Willey 2002
3. Sloss, Andrew, D. Symes, and Chris Wright. ARM system developer's guide: designing and optimizing system software. Morgan Kaufmann Publication, 2004.
4. P. J. Ashenden Digital Design: An Embedded Systems Approach Using Verilog, Morgan Kaufmann Publication, 2008.