	National Institute of Technology Meghalaya An Institute of National Importance	**CURRICULUM**

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution			
		L	T	P	C	INT	MID	END	Total
EC 532	**VLSI TESTING AND TESTABILITY**	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**200**

Course Objectives		Course Outcomes		
	Understanding testing methodology and testing		CO1	Able to programme for testing
	Study various faults in digital circuits		CO2	Able to detect faults and identify sources of faults
	Learn automation tools for testing		CO3	Able to realize BIST and JTAG Tests
			CO4	Able to integrate test to complex SoC system

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs		
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	CO1	**1**	**1**	**2**	**1**	**2**	**1**	**-**	**-**	**2**	**-**	**2**	**1**	**3**	**3**	**1**
2	CO2	**3**	**2**	**3**	**3**	**1**	**3**	**1**	**-**	**3**	**3**	**3**	**1**	**2**	**3**	**2**
3	CO3	**3**	**3**	**3**	**3**	**2**	**2**	**-**	**1**	**0**	**-**	**1**	**2**	**3**	**3**	**3**
4	CO4	**1**	**2**	**3**	**0**	**2**	**2**	**2**	**-**	**2**	**1**	**-**	**1**	**1**	**1**	**3**

SYLLABUS

No.	Content	Hours	COs
I	Introduction to Fault Modeling Difference between testing, fault diagnosis and verification. Physical faults and their modelling: stuck-at faults, bridging faults, CMOS stuck-open and stuck-on faults. Fault collapsing: fault equivalence and fault dominance	5	CO1
II	Logic and Fault Simulation Logic simulation techniques: compiled code, event-driven simulation. Fault simulation techniques: parallel, deductive and concurrent fault simulation, critical path testing. Fault models, fault detection and redundancy, fault equivalence and fault location, fault dominance, automatic test pattern generation	8	CO2
III	Test automation and Design verification Deterministic test generation for combinational circuits: Boolean difference method, path sensitization method, D-algorithm, PODEM, etc. Exhaustive and pseudo-exhaustive test pattern generation. Pseudo-random test pattern generation. Linear feedback shift register (LFSR), characteristic polynomial. Weighted random pattern generation. Test generation for sequential circuits: time frame expansion method	10	CO2
VI	Design for Testability (DFT) Test pattern generation for sequential circuits: adhoc and structured techniques. Scan path and level sensitive scan design (LSSD). Boundary scan (JTAG) standard.	8	CO3
V	Built-in Self-test (BIST) BIST for testing of logic and memories, Test automation, Design verification techniques based on simulation, analytical and formal approaches. Response compression techniques: ones count compression, transition count compression, signature compression. Aliasing and effects on fault coverage. BIST architectures: BILBO, STUMPS, etc	7	CO4
	Total Hours	38	

Essential Readings

1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 199

Supplementary Readings

1. T. Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000
2. N. H. E. Weste and D. Harris, Principles of CMOS VLSI Design, Addison Wesley, 3 rd Edition, 2004