	National Institute of Technology Meghalaya An Institute of National Importance		CURRICULUM

Programme	**Master of Technology in VLSI and Embedded Systems**	Year of Regulation	**2018-19**
Department	**Electronics and Communication Engineering**	Semester	**II**

Course Code	Course Name	Credit Structure				Marks Distribution		
		L	T	P	C	Continuous Evaluation	VIVA	Total
EC 560	**Memory Technologies &Testing Lab**	**0**	**0**	**2**	**1**	**70**	**30**	**100**

Course Objectives	Design of SRAM	Course Outcomes	CO1	Able to learn the design of a SRAM cell
	Design of DRAM		CO2	Able to learn the design of a DRAM cell
	Design and analysis of a complete memory		CO3	Able to design a complete memory block

No.	COs	Mapping with Program Outcomes (POs)												Mapping with PSOs			
		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3	PSO4
1	CO1	3	3	0	1	0	0	0	0	2	0	0	0	3	0	0	3
2	CO2	3	3	3	1	0	0	0	0	2	0	0	0	2	0	0	2
3	CO3	2	3	3	1	2	0	0	0	0	0	0	0	2	3	3	2

SYLLABUS			
No.	Content	Hours	COs
I	1. Design and analysis of a SRAM cell	3	CO1
	2. Design and analysis of a DRAM cell	3	CO2
	3. Design a complete 4 x 4 memory block	12	CO3
	4. Testing 4 x 4 memory block	8	CO3
	Total Hours	26	

Essential Readings

1. A. K. Sharma, Semiconductor Memories: Technology, Testing and Reliability, Wiley IEEE Press, 1997.

2. A. K. Sharma, Advanced Semiconductor Memories: Architectures, Design and Applications, Wiley- IEEE Press, 2003.

3. W. D. Brown, and Joe Brewer, Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices, Wiley-IEEE Press, 1997.

Supplementary Readings

1. J. Brewer, Nonvolatile Memory Technologies with Emphasis on Flash: A Comprehensive Guide to Understanding and Using Flash Memory Devices, Manzur Gill, Wiley-IEEE Press, 2008.

1. J.-P. Colinge, FinFETs and Other Multi-Gate Transistors Springer, 2008.

2. Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998.