Patron

Prof. B B Biswal, Director, NIT Meghalaya

Organizing Chair

Dr.Anup Dandapat, NIT Meghalaya SMDP Coordinator

Convenors

Dr.P.Rangababu, NIT Meghalaya ECE Dept

Dr.Surmila Thokchom , NIT Meghalaya CSE Dept

Members:

Faculties of EC Dept NIT Meghalaya
Faculties of CS Dept NIT Meghalaya

Experts/Resource Persons

Expert from IITs, NIT, CFTIS, NIELIT Calicut and industry

Who Can Register?

Faculty members of the technical institutions, Industry People, Research and PG scholars

Important Dates

Last date of application received	**12th Sep 2021**
Intimation of participation	**14th Sep 2021**

How to Register

Interested participants may apply through online registration in link https://nitm.ac.in/events/workshop_on_smdp-custom-ic-design on or before 014th Sep 2021.

- ***No registration fee*** will be charged from the participants.
- The number of participants is limited to 200.
- Participant's registration will be confirmed on first come first serve basis. Certificate will be issued to those participants who attend all the sessions online

Contact:

Dr.P.Rangababu, Department of Electronics and Communication, NIT Meghalaya, Shillong,
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Online National Workshop Programme

on

"Custom IC Design from Simulation and Verification to Tape-out"

16th – 20th Sept 2021

Sponsored by:

Special Manpower Development Programme

Organized by

Department of Electronics and Communication Engineering

&

Department of Computer Science and Engineering

National Institute of Technology Meghalaya

Venue

National Institute of Technology Meghalaya,
Bijni Complex, Laitumkhrah, Shillong, –793003

Course Objective

A modern custom IC chip is complex in nature; billions of transistors, millions of logic gates deployed for computation and control, along with large storage memories. How do engineers/researchers manage to design and verify these chips? Recent years have seen an increasing job market towards the Custom VLSI Design includes Physical design, Verification, Testing, Timing domains. Working in these domains requires deep understanding of concepts and hands-on experience of Industry relevant chip design and verification skills on EDA Tools. This workshop focused on training the participants the (students/faculties/scholars/engineers) on the custom IC design, programming, and verification etc.

About NIT Meghalaya

National Institute of Technology Meghalaya was established in the year 2010 as joint venture of Govt. of India and Govt. of Meghalaya with granted permanent campus of around 450 acres at Shora Cherrapunjee. The institute is functioning in its temporary campus at Shillong in East Khasi Hills district of Meghalaya and is about 2 Kms from the main bus stand of Shillong on Police bazaar – Laitumkhrah roadway. The city of Shillong is well connected with rest of country by road. The nearest railway station is at Guwahati (Assam), at a distance of 90 Kms from Shillong. The nearest airport is within city (15 Kms). The place has healthy climate with temperature ranging from 07°c to 16°c during December and is at an altitude of 1520 meters.

The Department of Electronics and Communication Engineering and Computer Science and Engineering was established in the year 2010. The Department offers B. Tech, M.Tech and Ph.D. programmes. The departments are well equipped with laboratories, computers, latest simulation softwares and our students are exposed to recent technologies and techniques. The departments have well experienced and dedicated faculty members with different research specializations in Microelectronics, VLSI Design and Embedded Systems, Communication, Digital Processing, RF Design Machine learning, Cryptography, and Internet of Things etc

Program Contents

- RTL Design
- FPGA Design
- Verification and Testing
- Physical Design
- Memory Design
- Timing Closure
- Machine learning hardware accelerator
- RISC -5 Processor Design
- Internet of Things

National Institute of Technology Meghalaya, Bijni Complex, Shillong-793003

Course Schedule

Dates	9.30AM to 11:00AM	11:05 AM to 11.25 AM	11.30 AM to 12:30 PM	12.45 PM to 2:00 PM	2:00 PM to 3.00 PM 3:00PM to 3:45 PM	3.45 PM to 5:00 PM	4:00 PM to 4:45 PM 4:45 PM to 5:30 PM
16.09.2021 (Thursday)	Registration and Inauguration & **Session 1** Intelligent sensors Prof: Ganapathi Panda	Tea	**Session 2** Intel FPGAs and Quartus tool flow Intel, Dr.Padmanaban	Lunch	**Session 3a** New Architecture Paradigms Dr.Samrat L.Sabat , UOH **Session 3b** Customized efficient Arithmetic Architectures Dr.P.Saha, NITM	Tea	**Session 4** MEMS-CMOS integrated Sensors Dr.Pradeep Rathore NITM
17.09.2021 (Friday)	**Session 4** Modelling of IoT and AI-based applications- in Academic, Agriculture, Health care, Tourism and Waste Management etc. from Dr. Y. Jayanta Singh NIELIT Guwahati	Tea	**Session 5** Timing closure on Intel FPGA by Intel Dr.Padmanaban	Lunch	**Session 6a** RISC -5 Processor: A Big Picture Shri.Hari Nagarajun TCS **Session 6b** Hardware accelerators on FPGA Dr.P.Rangababu, NITM	Tea	**Session 7a** Talk by Kaustub Shukla **Session 7b** Memory Design Dr.Anup Dandapat NITM
18.09.2021 (Saturday)	**Session 8a** ASIC Design and Verification Introduction-I Dr. Jayaraj U Kidav, NIELIT Calicut	Tea	**Session 8b** ASIC Design and Verification -II Dr. Jayaraj U Kidav, NIELIT Calicut	Lunch	**Session 9a** Functional Verification –1 Dr. Jayaraj U Kidav, NIELIT Calicut	Tea	**Session9b** Functional Verification –2 Dr. Jayaraj U Kidav, NIELIT Calicut
19.09.2021 (Sunday)	**Session 10a** FPGA Prototyping –Demo with Industry Standard Tools-I Mr. Sreejeesh SG NIELIT Calicut	Tea	**Session 10b** FPGA Prototyping –Demo with Industry Standard Tools-II Mr. Sreejeesh SG NIELIT Calicut	Lunch	**Session 11a** ASIC Design Flow – Description about Tools and its Demo (RTL to GDSII) Mr. Sreejeesh SG NIELIT Calicut	Tea	**Session 11b** ASIC Design Flow – Description about Tools and its Demo (RTL to GDSII) Mr. Sreejeesh SG NIELIT Calicut
20.09.2021 (Monday)	**Session 12a** IoT Applications on FPGA using RISC V Mr. Rajesh M NIELIT Calicut	Tea	**Session 12b** IoT Applications on FPGA using RISC V Mr. Rajesh M NIELIT Calicut	Lunch	**Session 13a** Linux Porting on RISC Mr. Rajesh M NIELIT Calicut	Tea	**Session 13b** Linux Porting on RISC Mr. Rajesh M NIELIT Calicut